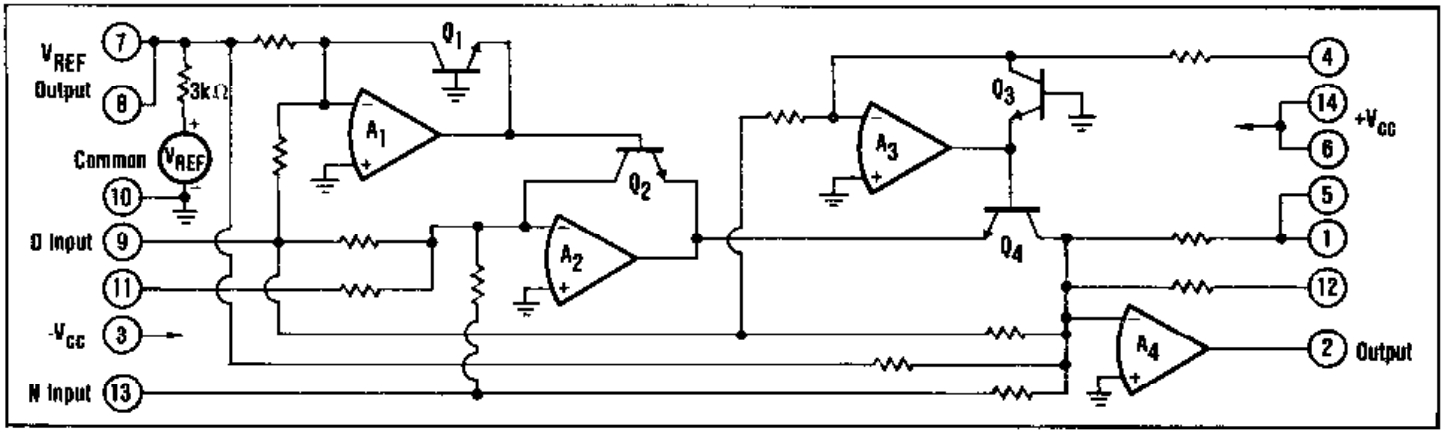
Analogdividierer DIV100

Der DIV100 logarithimiert die Eingangsspannungen, subtrahiert und exponenziert wieder

Die Schaltung



Blockdiagramm

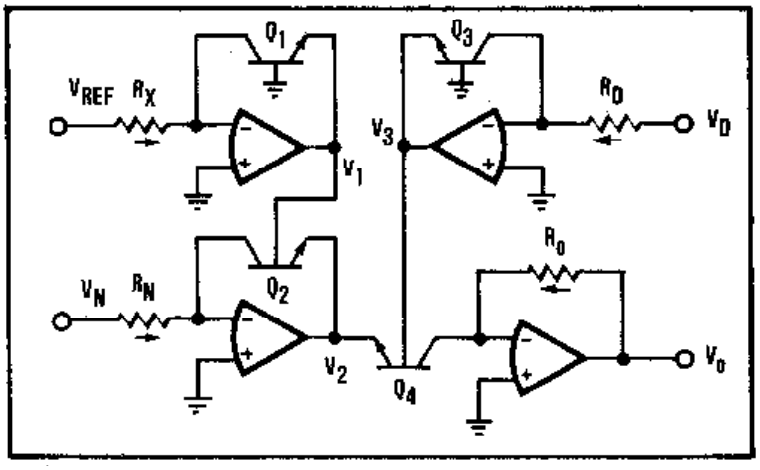


FIGURE 4. One-Quadrant Log-Antilog Divider.

Radizierer

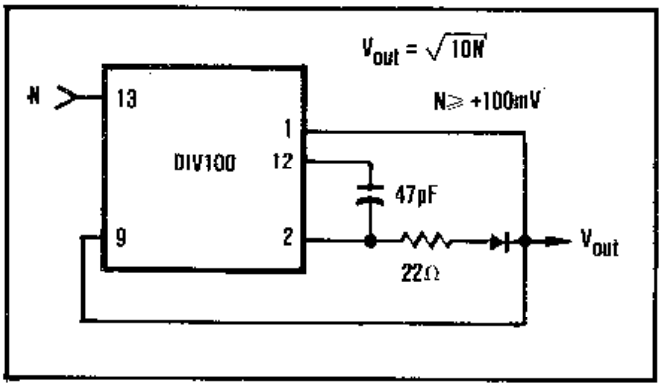


FIGURE 17. Connection for Square Root Mode

Brücken Linearisierung

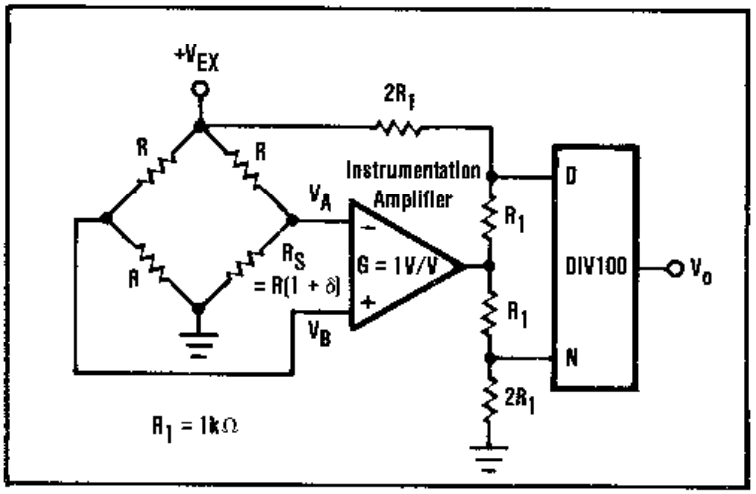


FIGURE 14. Bridge Linearization Circuit.

Spannungsgesteuertes Filter

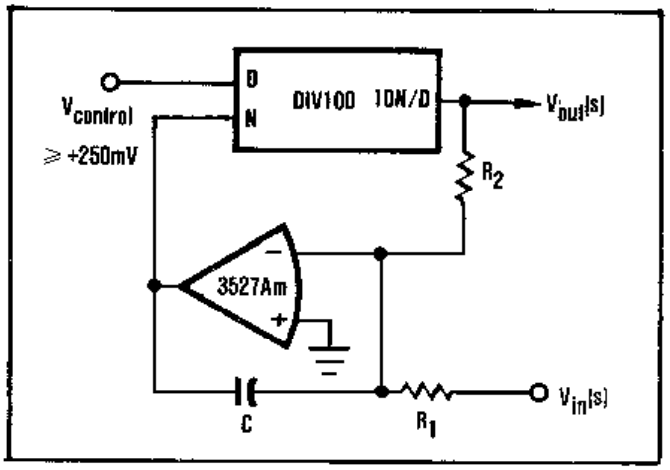


FIGURE 16. Voltage - Controlled Filter.

SPECIFICATIONS DIV100

Specifications at T_A = +25°C and $\pm V_{CC}$ = 15VDC unless otherwise noted.

MODEL		DIV100JP			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
TRANSFER FUNCTION			$V_O = 10N/D$		
ACCURACY	$R_L \geq 10k\Omega$				
Total Error					
Initial	$0.25V \leq D \leq 10V$, $N \leq \lvert D \rvert$		0.3	0.5	% FSO(1)
vs. Temperature	$1V \leq D \leq 10V$, $N \leq \lvert D \rvert$		0.02	0.05(2)	% FSO/°C
	$0.25V \leq D \leq 1V$, $N \leq \lvert D \rvert$		0.06	0.2(2)	% FSO/°C
vs. Supply	$0.25V \leq D \leq 10V$, $N \leq \lvert D \rvert$		0.15		% FSO/%
AC PERFORMANCE	D = +10V				
Small-Signal Bandwidth	-3dB		350		kHz
0.5% Amplitude Error	Small-Signal		15		kHz
0.57° Vector Error	Small-Signal		1000		Hz
Full-Power Bandwidth	$V_O = \pm 10V$, $I_O = \pm 5mA$		30		kHz
Slew Rate	$V_O = \pm 10V$, $I_O = \pm 5mA$		2		V/μsec
Settling Time	$\epsilon = 1\%$, $\Delta V_O = 20V$		15		μsec
Overload Recovery	50% Output Overload		4		μsec
INPUT CHARACTERISTICS					
Input Voltage Range					
Numerator	$N \leq \lvert D \rvert$	±10			V
Denominator	$D \geq +250mV$	+10			V
Input Resistance	Either Input		25		kΩ
POWER SUPPLY REQUIREMENTS					
Rated Voltage			±15		VDC
Operating Range	Derated Performance	±12		±20	VDC
Quiescent Current					
Positive Supply			5	7(2)	mA
Negative Supply			8	10(2)	mA
AMBIENT TEMPERATURE RANGE					
Specification		0		+70	°C
Operating Range	Derated Performance	-25		+85	°C
Storage		-55		+125	°C